DESIGN CONSIDERATIONS AND PERFORMANCE REQUIREMENTS FOR HIGH SPEED DRIVER AMPLIFIERS

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1. INTRODUCTION

The requirements for high speed driver amplifiers present a tough challenge to circuit designers. The two key requirements are a very broad instantaneous bandwidth and very good phase linearity. Allied to the broad band requirement is the need for constant gain and output power with frequency. Achieving all of these simultaneously requires careful consideration and understanding of the issues involved. In this technical note we take a general look at the background to these requirements and circuit techniques used by engineers at LA Techniques to achieve them for data rates beyond 10 Gb/s.

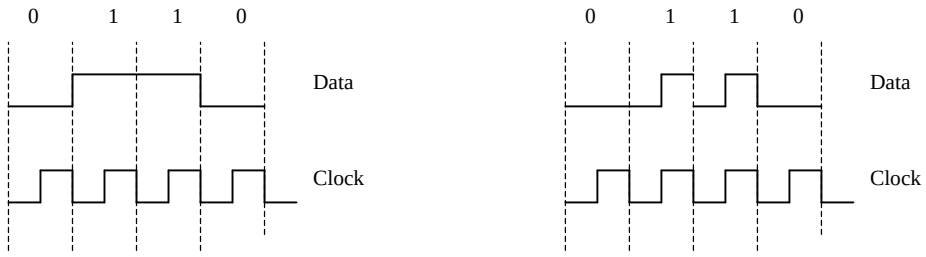
2. THE RANDOM DIGITAL SIGNAL – BANDWIDTH REQUIREMENTS

Driver amplifiers are required to handle digital signals carrying encoded data. Generally, this data will have random or noise like characteristics. That is, the likelihood of transmission of a ‘1’ at any time is the same as that of a ‘0’. Given this situation, it is not difficult to imagine that the digital data signal can contain long strings of consecutive 1s or 0s or a long pattern of 1s and 0s that may repeat a few times. Therefore, looking at the distribution of power in the frequency domain, it is clear that the digital signal can have components at very low frequencies as well as components at and beyond the raw bit rate. So, given this situation, it follows that a driver amplifier must be able to handle all frequency components without distortion in order to faithfully reproduce the digital signal.

The exact power spectrum of a digital data signal will depend on the transmission format employed and any encoding used. Data encoding is generally used to add redundancy to the signal in order to allow error detection and correction. This process usually breaks the data into packets for better efficiency and ease of handling. There are two popular techniques for the transmission of high speed digital signals. These are non-return to zero (NRZ) and return to zero (RZ). In the following section we look at the differences between these and their power spectra.

3. NRZ AND RZ SIGNALS

Non-Return to Zero (NRZ) and Return to Zero (RZ) are two transmission formats for high speed digital data. Figure 1 below shows the idealised time domain characteristics of each.



(a) NRZ (b) RZ

Figure 1. Ideal NRZ and RZ characteristics

NRZ

This is the most basic format for digital data. In this a logic ‘1’ is represented by a high signal level lasting a clock period. The frequency spectrum of a 10 Gb/s data stream is shown in Fig. 2 below. The key feature to note is that a null exists at 10 GHz, the clock frequency, and most of the energy is contained below 10 GHz. From this we can understand that it should be possible to transmit 10 Gb/s NRZ data over a circuit bandwidth less than 10 GHz without excessive distortion. Also, an interesting side issue is the absence of a clock component (10 GHz in the example). This means that recovering and re-timing the data requires special non-linear techniques such as frequency doubling.

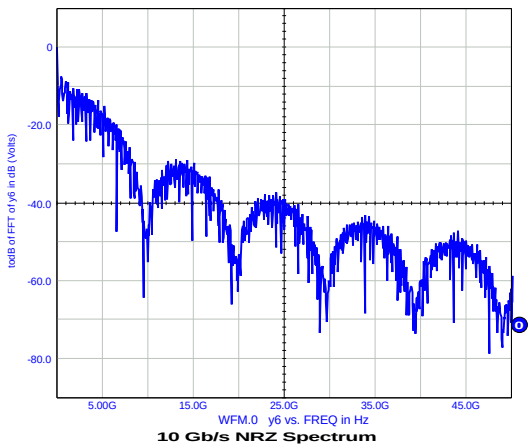


Figure 2. Bandlimited NRZ Data Power Spectrum

RZ

Return to zero data can be obtained by simply combining NRZ data and the data clock in an AND gate. Putting it simply, the result is a '1' for half the clock period for the symbol '1' and a '0' for the entire clock period for the symbol '0'. This technique is attractive in some situations as it can be more efficient for the transmission of the optical signal [Ref.2]. The simulated time domain and frequency characteristics of a band limited, 10 Gb/s random data stream are shown below in Figs. 3 and 4.

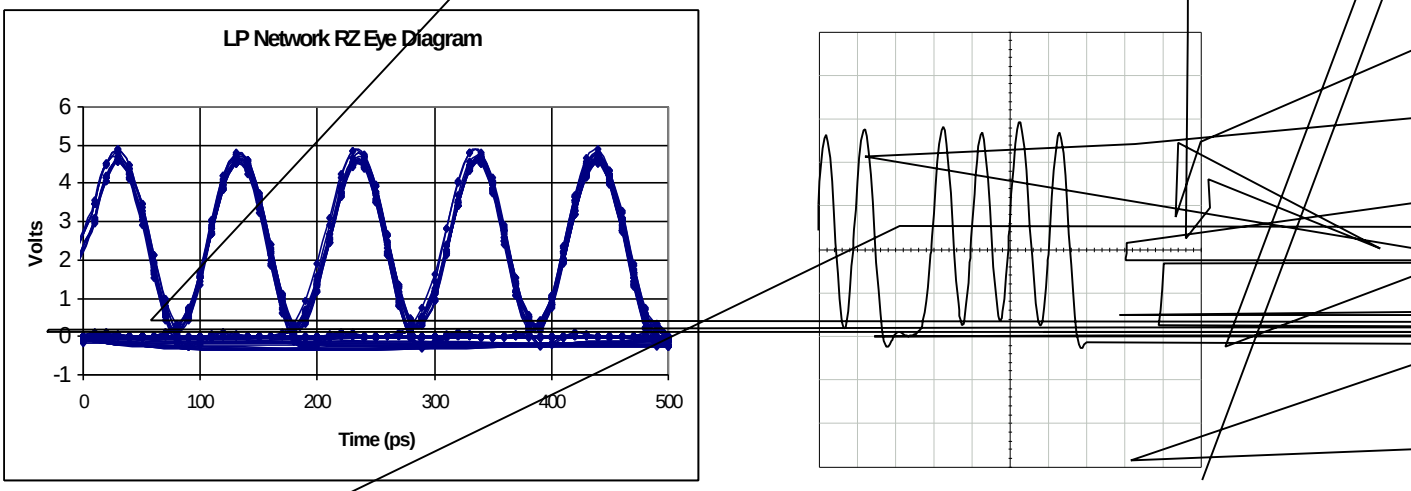


Figure 3. 10 Gb/s Bandlimited RZ Characteristics

Figure 4. 10 Gb/s RZ Data Power Spectrum

It can be seen that the RZ signal contains significant energy above 10 GHz. This is in contrast with the NRZ situation where a null exists at 10 GHz and energy above this decays fairly rapidly. This means that a considerably broader bandwidth is required to pass RZ data without distortion. Typically, depending on the exact system

requirements, this amounts to between 15 and 25 % more bandwidth than that for NRZ data. Another feature of RZ data is that there exists significant energy at the clock frequency (10 GHz in the example) thereby easing the requirement of data recovery and re-timing.

4. CIRCUIT TECHNIQUES

It is clear from the previous sections that any amplifier used to pass high speed, random digital data must have a very broad instantaneous bandwidth. This means an amplifier with a very good amplitude and phase response over a very broad band. The latter refers to the insertion phase linearity, that is, its deviation from a linear phase response.

Phase linearity is often presented in the form of group delay. This is the rate of change of phase with frequency and is defined as follows.

$$GD = \frac{\partial f}{\partial w}$$

Where ϕ is the insertion phase in radians and ω is the frequency of operation in radians per second.

Group delay is generally useful in providing an idea of the overall quality of the phase linearity, however it can sometimes be misleading, giving an over-pessimistic impression of performance. This is illustrated in Fig. 5 below. Here a very small, but fast, change in absolute phase can lead to a large variation in group delay. If the amplifier is specified in terms of peak to peak group delay variation, then this can be a problem. In reality a small perturbation over a narrow band in the phase response will not be significant. This is different from other situations such as microwave radio links where phase distortion over a small part of the band can be very damaging. Qualitatively, this is the case because the useful information in our situation is spread over an extremely large bandwidth. This contrasts with microwave radio links where useful data can be concentrated over a very narrow bandwidth.

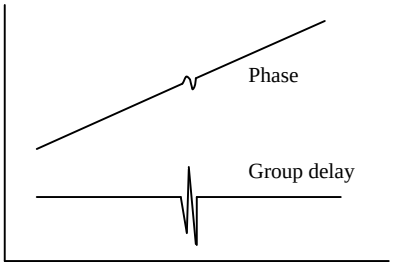


Figure 5. A small perturbation in insertion phase can lead to significant group delay variation

Generally, it is more useful to show and specify the phase response of the amplifier in terms of departure from linear phase in degrees. This provides a clearer idea of the relative phase shift of the various frequency components relative to one another. A rough guide is that, for example, for 10 Gb/s operation, 10^O – 20^O up to 10 GHz can be tolerated, and for best rise time performance this needs to be extended to 15 GHz.

In the following sections two popular circuit techniques used to implement wide band amplifiers are discussed. The first is feedback which can provide a very power efficient solution, particularly in low to medium speed applications. For higher speeds the distributed amplifier topology is likely to provide the best approach.

4.1 The Feedback Amplifier

The general feedback amplifier topology is shown in Fig. 6 below. This is a conventional shunt feedback amplifier stage and can provide good performance up to several GHz using high frequency GaAs MESFET devices.

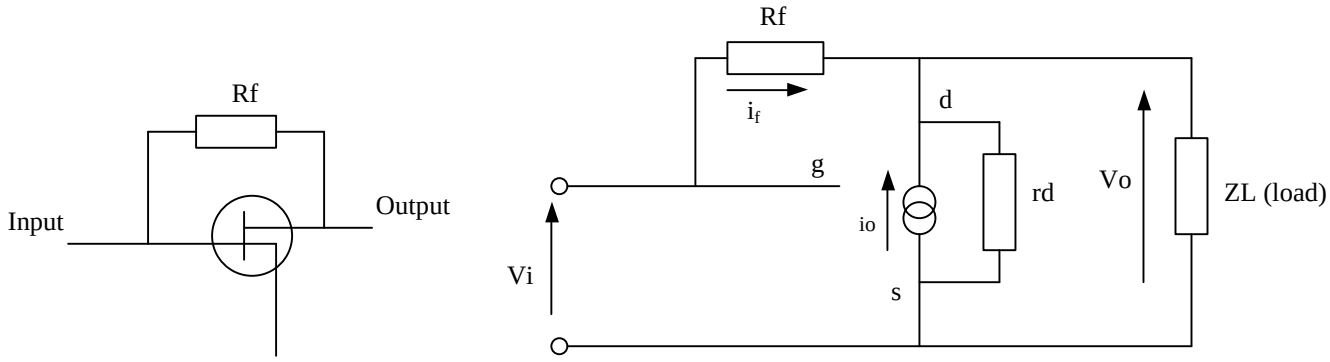


Figure 6: Simplified Feedback Amplifier Stage and its Equivalent Circuit

In order to illustrate the general approach, a simplified analysis of the amplifier is as follows.

$$Vo = (io + if)ZL \qquad \text{(1)}$$

$$io = -Vi.gm \qquad \text{(2)}$$

$$if = \frac{(Vi - Vo)}{Rf} \qquad \text{(3)}$$

Where g_m is the transconductance of the FET. The above assumes that rd >> ZL and disregards high frequency effects. Further, substituting (3) and (2) into (1) and re-arranging, we arrive at the expression for voltage gain as follows.

$$\frac{Vo}{Vi} = \frac{ZL - gm.ZL.Rf}{Rf + ZL}$$

= voltage gain, G

Similarly, we can use the above equations to derive an expression for the input resistance.

$$\frac{Vi}{if} = \frac{Rf + ZL}{1 + gm.ZL}$$

= input resistance, Zi

The output resistance can be estimated as follows;

$$Vi = \frac{Vo}{Rf + Zs}.Zs \qquad \text{\_\_\_\_\_(4)}$$

where,
Vi = the voltage at the gate terminal
Vo = the output voltage
Zs = the source resistance

Further,

$$io = Vi.gm \qquad \text{\_\_\_\_\_ (5)}$$

$$if = \frac{Vo}{Rf + Zs} \qquad \text{\_\_\_\_\_ (6)}$$

Also, disregarding rd, we have;

$$Zo = \frac{Vo}{io + if} \qquad \text{\_\_\_\_\_ (7)}$$

Re-arranging the above, we can derive an expression for the output resistance as follows.

$$Zo = \frac{Rf + Zs}{Zs.gm + 1}$$

= output resistance

Now, if we take, as an example, a medium power transistor with the following parameters;

gm = 80 mS

and assume Rf = 220Ω, ZL = 50Ω, and Zs = 50Ω; we end up with the following basic amplifier parameters;

Voltage gain:	-3.07	(inverting, approximately 9.7 dB power gain)
Zi:	54 Ω	
Zo:	54 Ω	

The above figures would provide an ideal amplifier stage with excellent input and output impedance characteristics. At the higher frequencies, where the feedback mechanism is no longer effective due to excessive phase shift through the transistor and low, effective transconductance, traditional microwave matching techniques can be applied to extend the useful bandwidth of the amplifier. Some care needs to be exercised to ensure phase linearity is retained.

The feedback amplifier can be used for fairly high power amplifier stages up to about 2.5 Gb/s operation (for example the LA Techniques amplifier LA32-03-02 uses this technique). For 10 Gb/s operation, feedback techniques are restricted to small signal handling since power transistors suffer excessive phase shift and gain roll-off at the higher frequencies. In this case the distributed amplifier approach is required.

4.2 The Distributed Amplifier

The basic idea of the distributed amplifier is quite old and was first proposed for use with thermionic valves for the purpose of extending operating bandwidth. The circuit topology lends itself well for use with FET devices and recent reported bandwidths exceed 100 GHz. The basic circuit arrangement is shown below in Fig. 7. This is a two stage amplifier for illustration purposes, in practice several more stages are normally used.

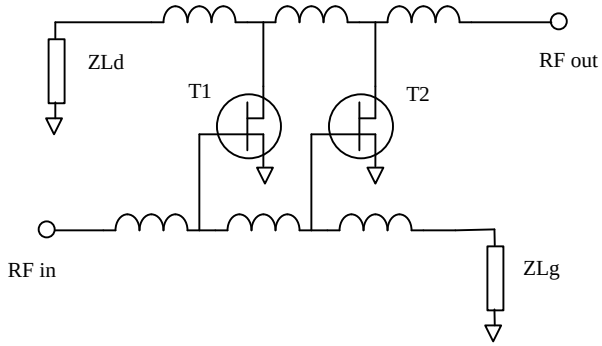


Fig. 7 Simplified Two Stage Distributed Amplifier

The basic principle of the techniques is to use the input (Gate) and output (Drain) capacitance of the FET to form two artificial transmission lines by the addition of lumped inductors. In Fig. 7 above, the input or Gate transmission line is terminated in load ZLg and the output or Drain transmission line is terminated in load ZLd.

The nominal impedance, frequency cut-off and time delay for the artificial transmission lines are given by the following expressions;

$$Zo = \sqrt{\frac{L}{C}}$$

$$fc = \frac{1}{p\sqrt{LC}}$$

$$\partial t = n\sqrt{LC}$$

In the above, n is the number of stages making up the transmission line, L is the lumped element inductance and C is the lumped element capacitance.

Signals arriving at the input terminal (RF in) travel down the Gate line and are dissipated in load ZLg. As the signal passes voltages are set up at each of the Gate terminals. This leads to a proportional Drain current to flow from each transistor. This current splits two ways. One half travels towards the main output port, RF out, and the other half travels towards the load ZLd. Sometimes, the node at which ZLd is connected is referred to as the Idle Drain port.

Now, if we arrange that the delay through each of the Gate line sections is the same as that through the Drain line sections, we have a situation whereby all the Drain current contributions from each transistor will arrive at the "RF out" port with the same phase. So, there is constructive addition of all the currents at the main output, RF out.

The ideal case distributed amplifier has a gain given by;

$$Gav = 0.25n\ g_m{}^2 Z_g Z_d$$

This indicates that the gain of the amplifier is proportional to the number of stages, the square of the transconductance of the FETs (g_m), the characteristic impedance of the Gate line (Z_g) and the characteristic impedance of the Drain line (Z_d). Given that it is desirable to make Z_g and Z_d 50 Ω to achieve a good match, and that g_m is a function of the FET selected, then the required gain can be set by adjusting the number of stages making up the amplifier. In practice, losses associated with the lumped elements and the transistors themselves play a significant part at high frequencies [1] and need to be taken into consideration.

The general case distributed amplifier gain characteristic is shown below in Fig.8. The forward gain, that is RF in to RF out, is frequency independent up to the cut-off frequency, f_c, of the artificial transmission lines. Beyond this point it rolls off at rate dependent on the number of stages used.

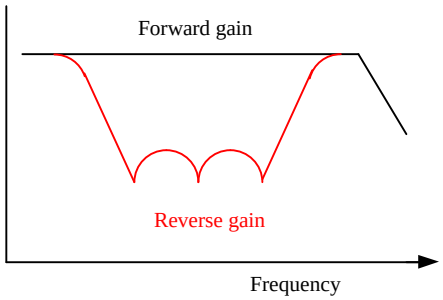


Figure 8. General Gain Characteristic of the Distributed Amplifier

The situation regarding the reverse gain is very different. The key here is that the contributions from the various transistors arriving at the idle Drain port do not arrive with the same phase. Further, the phase difference between the various components is frequency dependent as the insertion phase of the artificial transmission line stages are naturally frequency dependent. This leads to destructive addition of the signal, hence the characteristic shown in Fig. 8 above. Note that the only case when the reverse gain is the same as the forward gain over the entire band is in the single stage distributed amplifier.

The key advantages and disadvantages of the distributed amplifier can be summarised as follows;

Table 1.
Advantages and Disadvantages of the Distributed Amplifier

Advantages	Disadvantages
• Very broad band performance • Inherently good match • Power combining characteristics • Partially isolated port for dc bias injection	• Inefficient • Large component count

5. DESIGN CONSIDERATIONS

5.1 Technologies

There are various techniques available for implementing high speed driver amplifiers. Perhaps the most popular is the use of pre-matched MMIC (monolithic microwave integrated circuit) amplifier chips (distributed amplifiers) on an alumina substrate. This is a well proven and with good control processes, can yield a reliable product.

In addition to the conventional chip and wire techniques, there is also chip on board (COB) and conventional SMT (surface mount technology). COB has been used successfully in some of LA's products and its key advantage is in minimising the amount of expensive chip and wire content of the product. The propriety COB process

developed at LA accounts for thermal management in high power MMICs which is essential for the reliable operation of the driver amplifier.

6.2 Bias and Decoupling Techniques

Several techniques exist for applying the necessary dc bias to the active components. In the case where high currents are concerned a low loss component employing a ferrite inductor is normally applied. This needs careful design and special compensation circuitry to control any spurious resonance. In this respect the distributed amplifier offers a slight advantage in that the high current bias injection can be applied through the "idle drain" terminal. This provides a degree of isolation over a large part of the band thereby easing the task.

Where space is limited and distributed amplifier stages are used, it is possible to apply the bias current through the idle drain port 50Ω termination. Although this is inefficient and needs careful thermal management, it can provide good results without the large footprint needed for a proper bias-T circuit.

Decoupling

In applications operating at and beyond 10 Gb/s, efficient decoupling over the band in question (approximately 30 kHz to over 10 GHz) becomes a key issue in the design of driver amplifiers. In theory all that is required is the provision of a microwave capacitor in parallel with a high value, low frequency part. The former provides low loss at microwave frequencies and the high value part takes care of the low frequency performance.

In practice, the key problem is connecting the two capacitors in such a way that high Q parallel resonance does not occur. In general the high value capacitor will series-resonate at relatively low frequencies and appear inductive at microwave frequencies. This forms a parallel resonant circuit with the low value microwave capacitor which can lead to severe ringing in the response of the circuit. The basic idea is shown in Fig. 9.

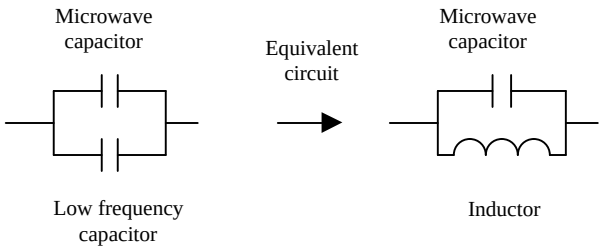


Figure 9. Basic Problem of Broadband Decoupling

This problem is generally overcome by LA Techniques by lowering the Q of the resonance, thereby minimising any phase and amplitude distortion to the signal.

Interfacing to Optical Modulators

The issue here is the potential load impedance mismatch. Clearly, the situation will vary according to the specific modulator in question but consideration needs to be given to the possibility of significant mismatch. For example, high performance 2.5 Gb/s modulators with an impedance of around 25Ω, resistive, are fairly common. In such situations, it is important that the output impedance of the driver amplifier is close to 50Ω, and remains so at all output level settings over the operating bandwidth. This allows reflections from the load (optical modulator) to be absorbed without any further reflections. Note that in our example, making the amplifier output impedance 25Ω would make the situation unless the connecting cable and interface hardware (RF connectors, etc.) could also be made 25Ω. Figure 10 shows the points at which reflections arise. If the Driver amplifier has a good output match (high return loss) then significant multiple reflections that can lead to eye degradation will not set up. In addition, it is important that the connecting cable has low dispersion in order to minimise distortion.

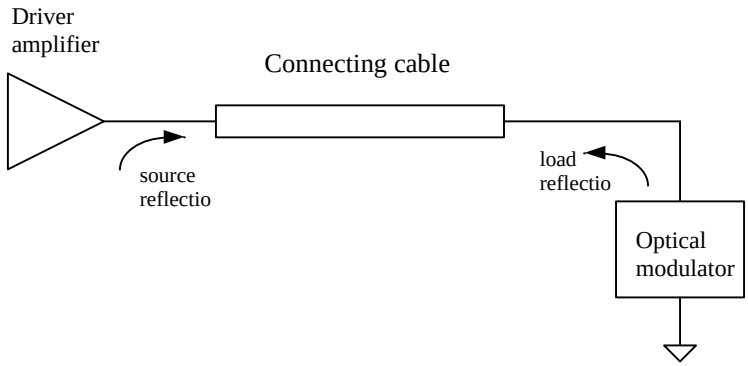


Figure 10. Possible Multiple Reflections
with an Optical Modulator Load

6. CONCLUSIONS

The key performance requirements necessary for high speed driver amplifiers have been described. In addition, an overview of the design techniques available for implementing high speed driver amplifiers has been presented. All of these techniques are or have been used on products from LA Techniques Ltd.

7. REFERENCES

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